# COAL-BASED IGFC PROJECT PHASE I

FC26-08NT0003894

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**12th Annual Solid State Energy Conversion Alliance (SECA) Workshop**
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Sheraton Station Square Hotel
Pittsburgh, PA

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# OUTLINE

- Summary of stack performance highlights from past year
- Cell and stack fabrication
- Gen 4 stack seal development
- Gen 4 stack voltage variation improvement
- Interconnect and contact material development
  - Constant current
  - Thermal cycling

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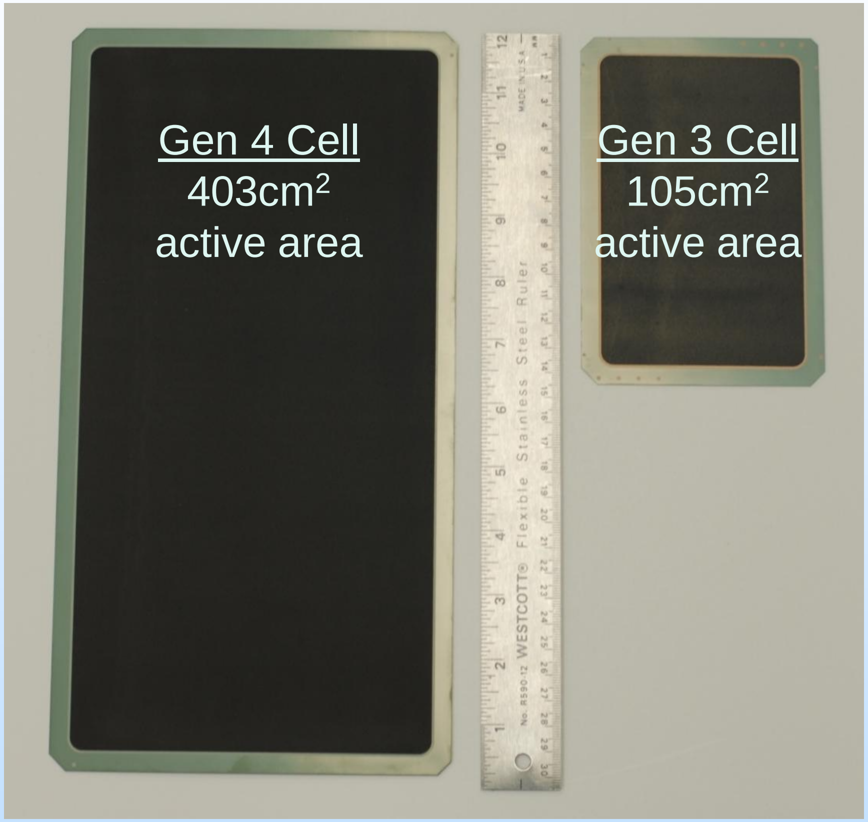
# SUMMARY OF SECA COAL BASED SYSTEM STACK DEVELOPMENT

- Completed scale up of cells from 105 $cm^2$ (active area) cells to 403 $cm^2$ for Gen 4 stacks
- Added additional Gen 4 stack fabrication and testing capabilities
- Fabricated and tested 24 Gen 4 stacks and 55 Gen 3 stacks in past year
- Completed Red X® investigations to improve stack sintering process and decrease stack voltage variation
- Demonstrated 7,000+ hours continuous durability on Gen 3.2 stack; demonstrated 5,000+ hours on Gen 4 stack.
- Completed 70 full thermal cycles on Gen 4 stack, with less than 5% voltage degradation

# CELL AND STACK FABRICATION

- Fabricated in past year
  - About 2,200 Gen 4-sized cells
  - 24 Gen 4 stacks of varied configurations (most 30-cells or greater)
  - 55 Gen 3 stacks of varied configurations (many 30-cells or greater)



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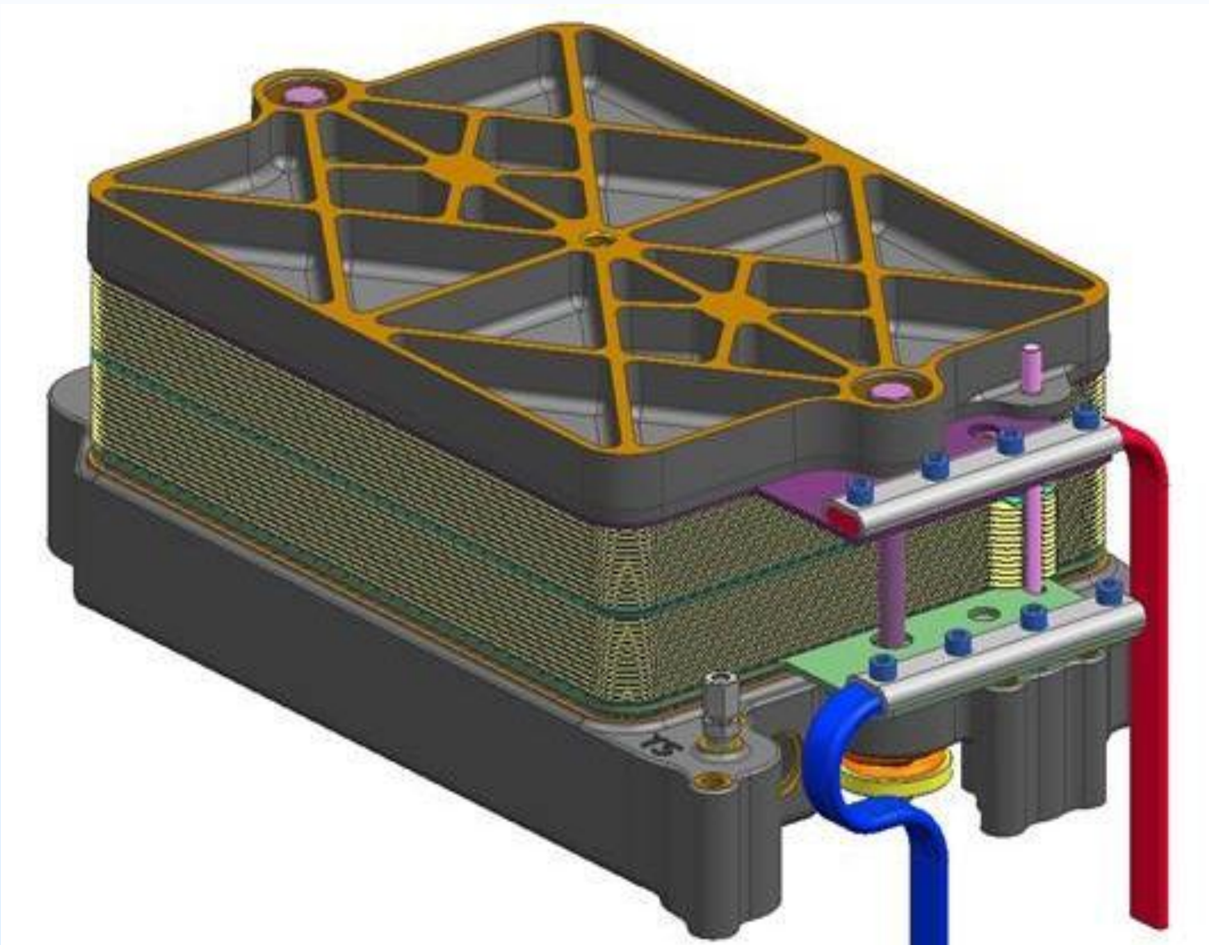
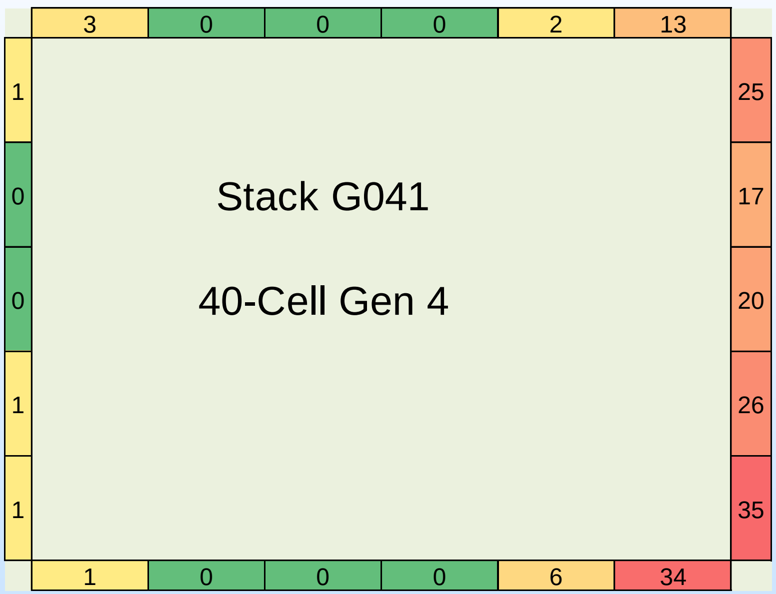
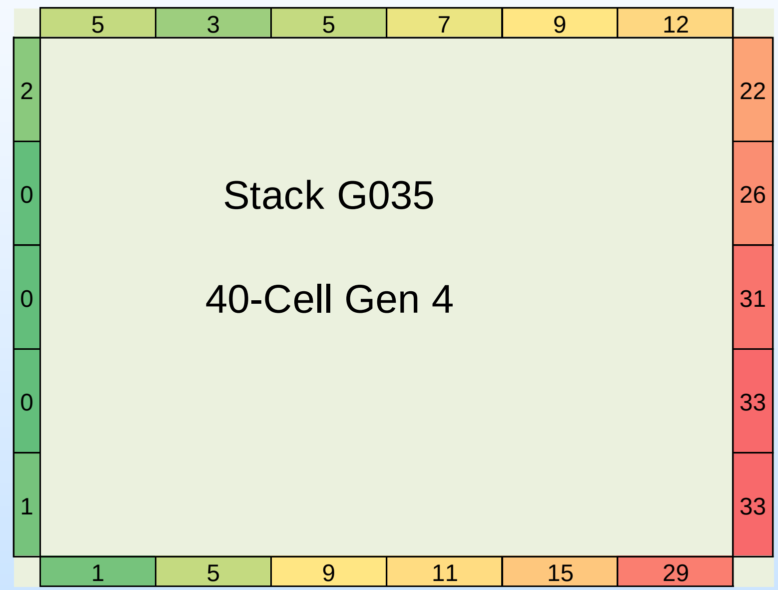
# GEN 4 STACK SEAL DEVELOPMENT PROJECT



Inlet Perimeter

# CONCENTRATION DIAGRAMS OF POROUS SEAL MICROSTRUCTURES



# STACK SINTERING OPTIMIZATION PROJECT

- Confirmed overheating of the stack seals
  - PNNL XRD analyses
  - Microstructural analysis
  - Coupon confirmation testing at increased sintering temperatures
- Teardown analyses of previous stacks
- Thermal mapped build stands and stacks during standard build process
- Developed strategy for investigating build control factors for improved thermal control during sintering
- Completed stack mapping thermal profiles with varied build controls
- Confirmation run with new build control parameters

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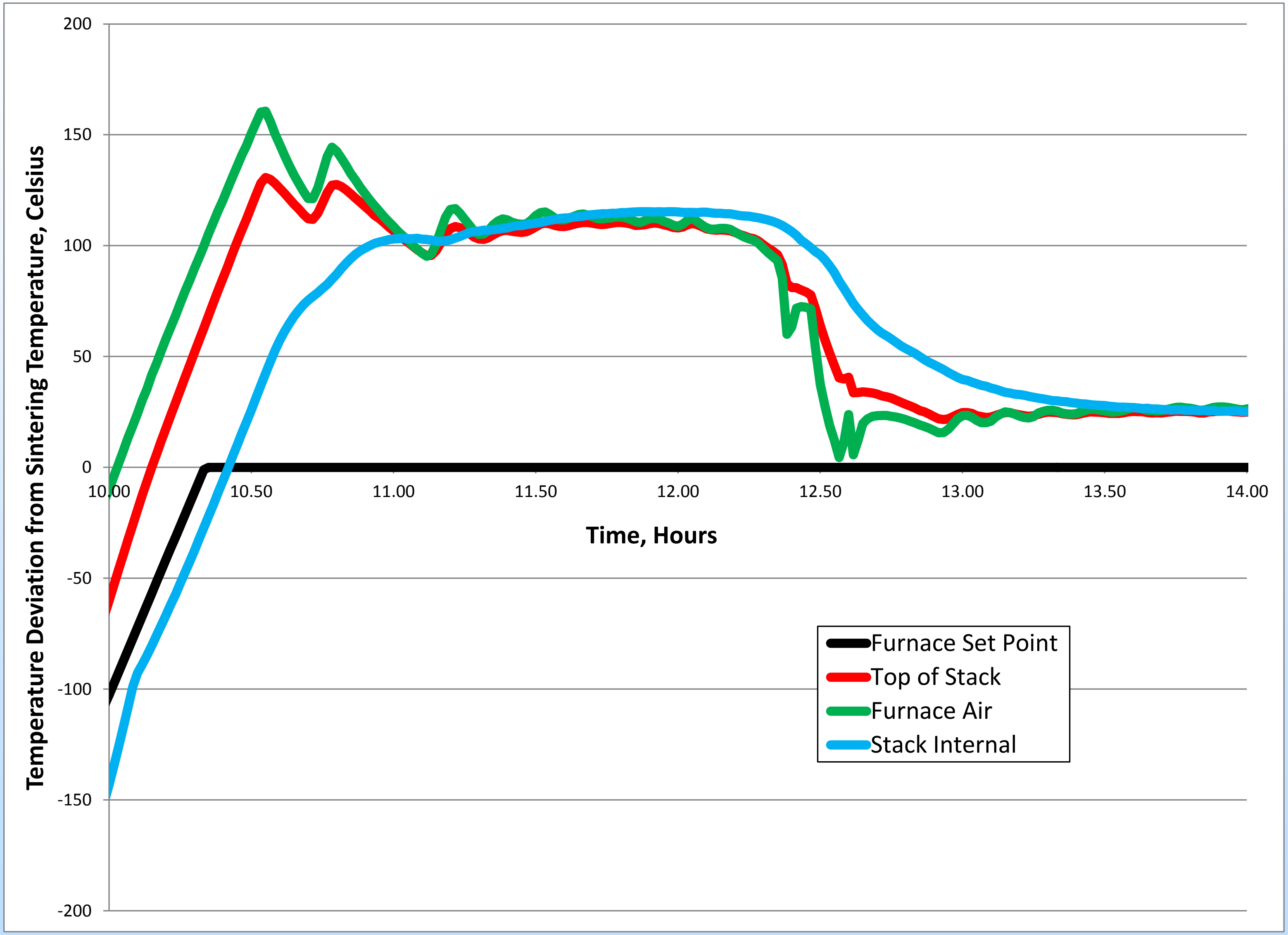
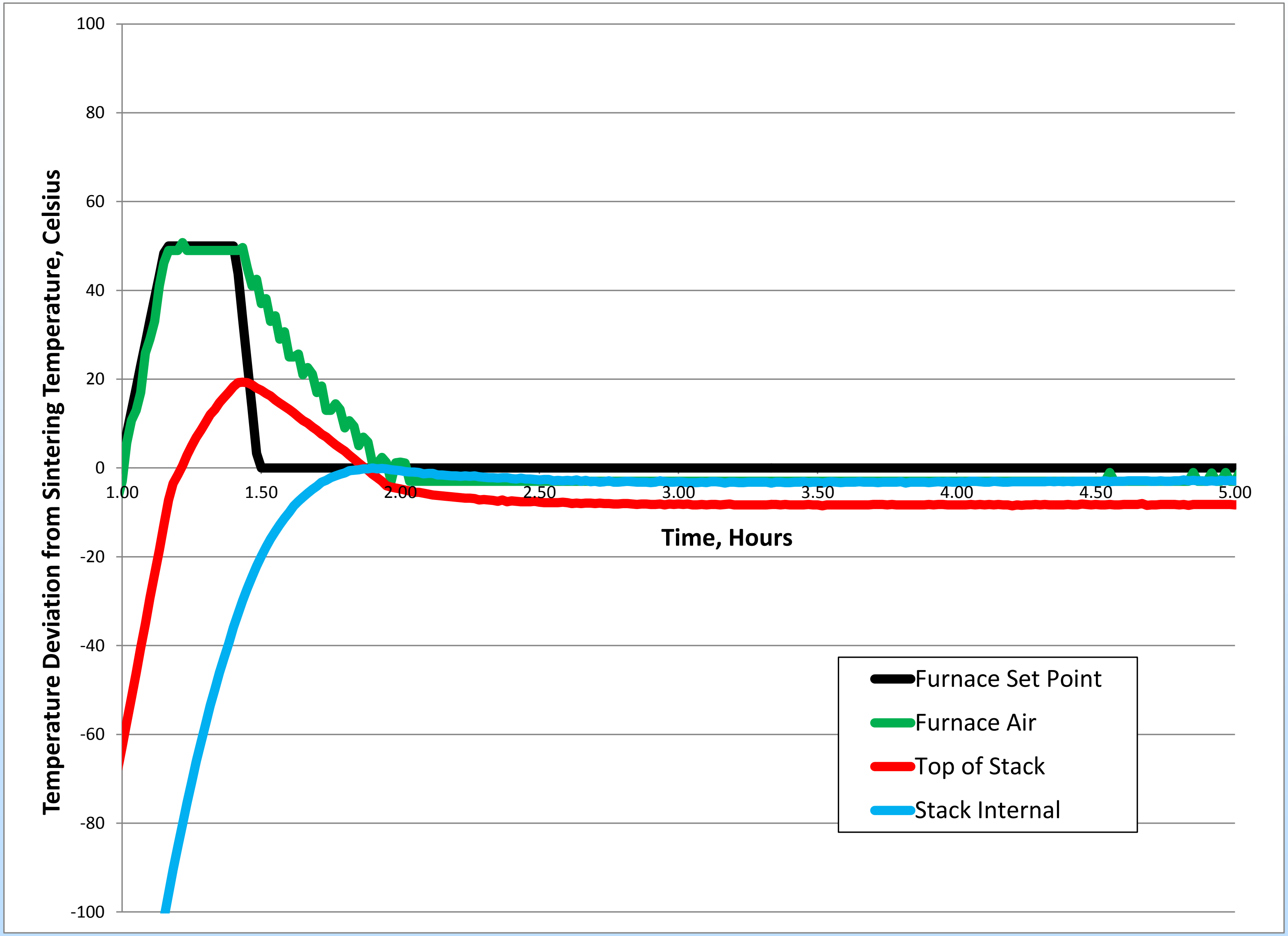
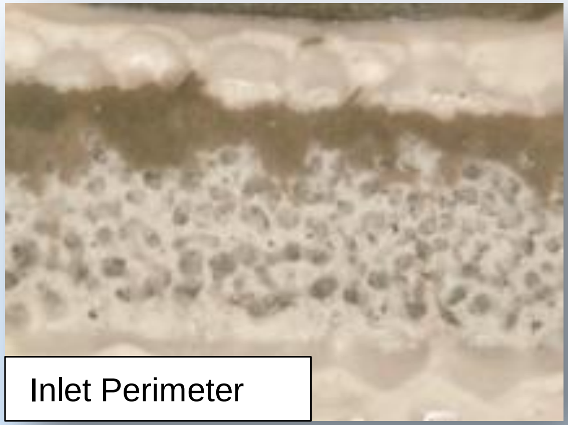
# TEMPERATURE PROFILES PRIOR TO OPTIMIZATION OF SINTERING CYCLE



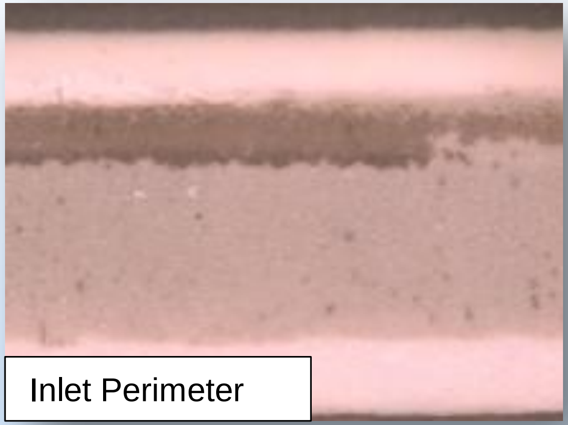
# TEMPERATURE PROFILES AFTER OPTIMIZATION OF SINTERING CYCLE



# SEAL STRUCTURAL IMPROVEMENT FROM SINTERING OPTIMIZATION

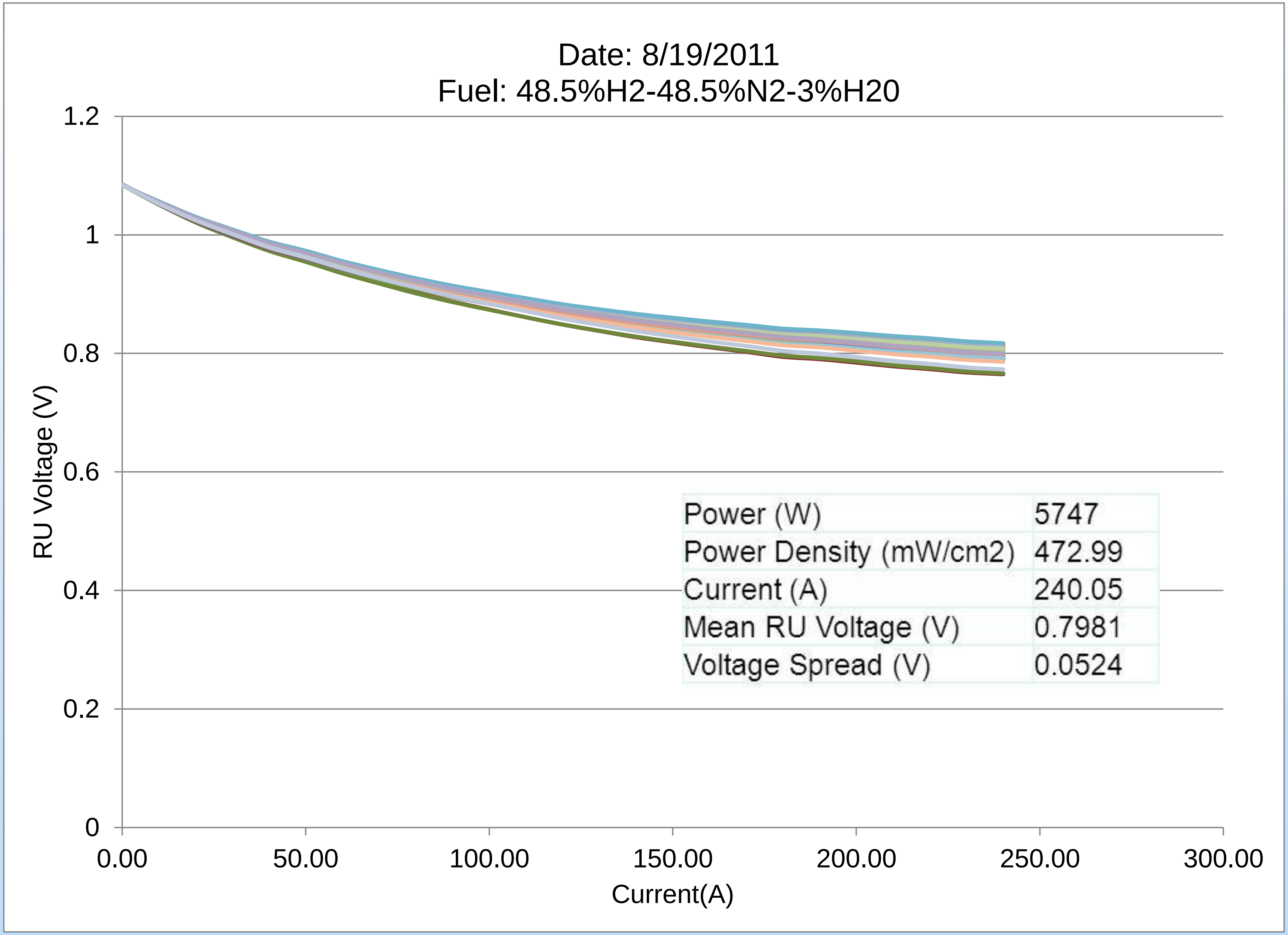



Stack Perimeter Seal Prior to Optimization of Sintering Cycle




Stack Perimeter Seal After Optimization of Sintering Cycle

# INITIAL GEN 4, 30-CELL STACK PERFORMANCE USING OPTIMIZED SINTERING PROFILE

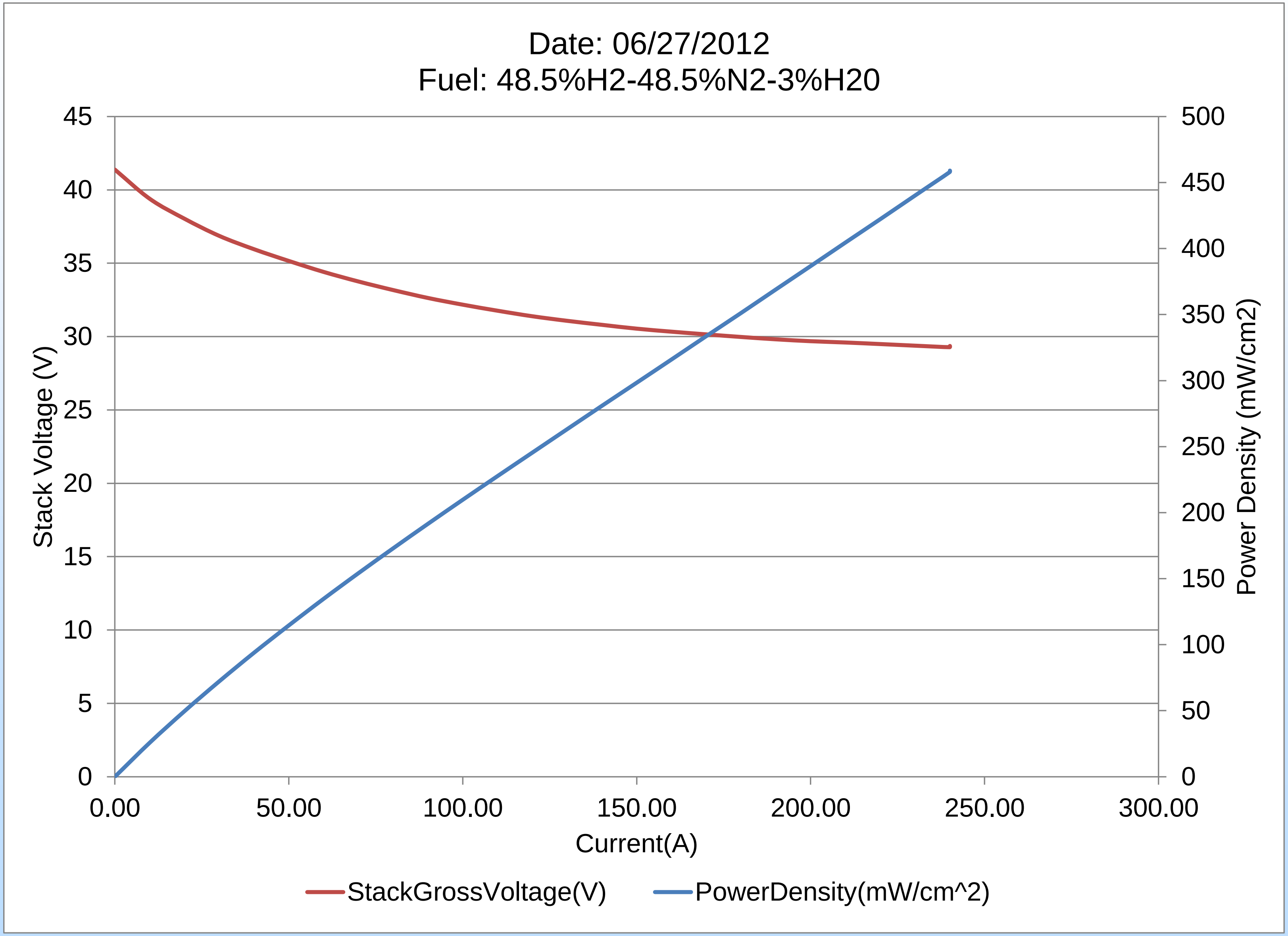



| | |
|---|---|
| Power (W) | 5747 |
| Power Density (mW/cm2) | 472.99 |
| Current (A) | 240.05 |
| Mean RU Voltage (V) | 0.7981 |
| Voltage Spread (V) | 0.0524 |

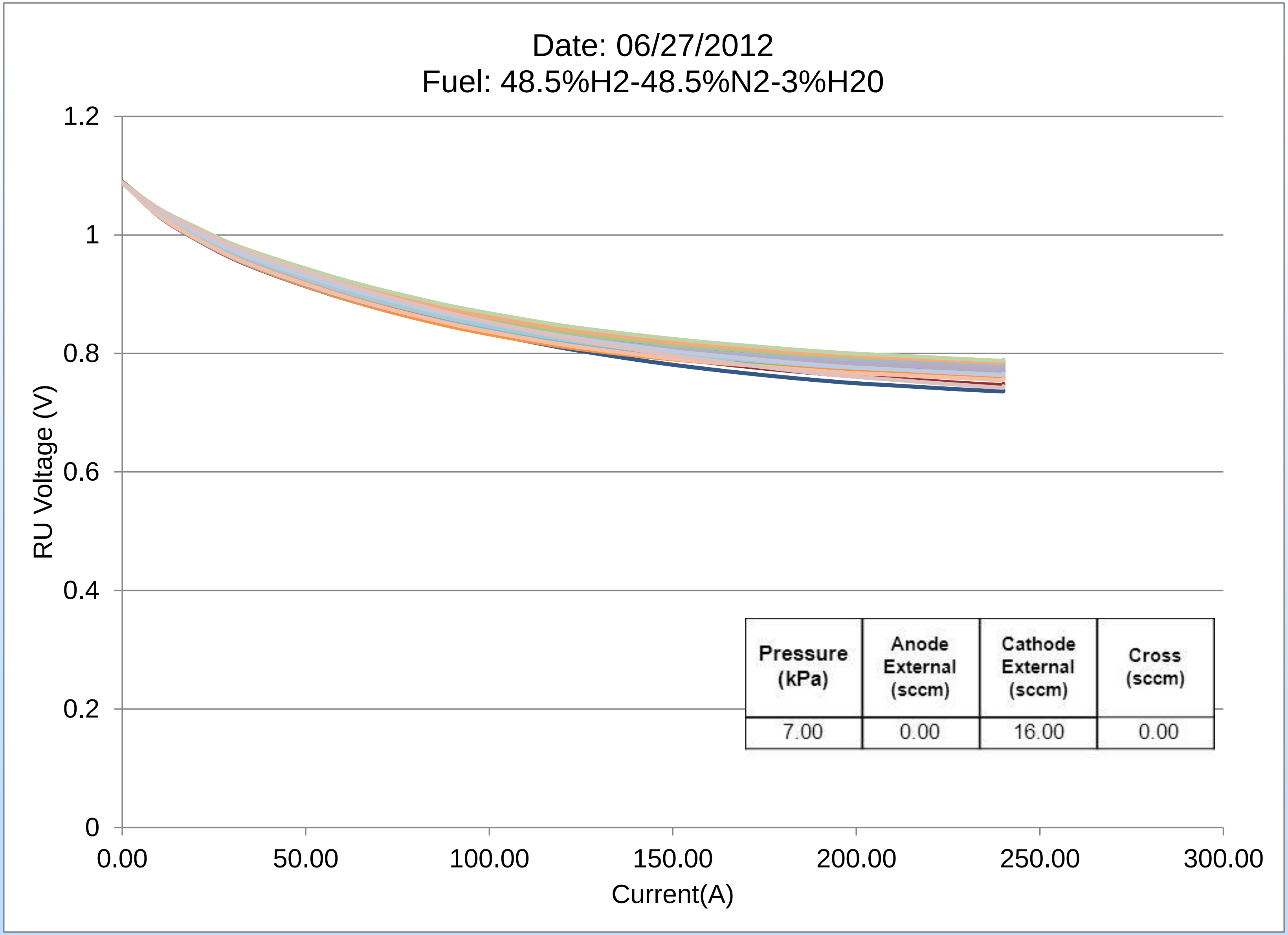
# RED X® STUDY ON MINIMIZING STACK REPEATING UNIT VOLTAGE VARIATION

- Analyzed numerous Gen 4 stacks
  - Cross sections
  - Repeating unit teardowns
  - X-ray and metallographic analyses of repeating units
  - Measurement studies of numerous repeating unit components
  - Optical and SEM inspection of components
- Conducted sintering studies
  - Component level
  - Full stack level

# MOST RECENT 38-CELL GEN 4 STACK INITIAL POLARIZATION PERFORMANCE AFTER RED X ® PROJECT

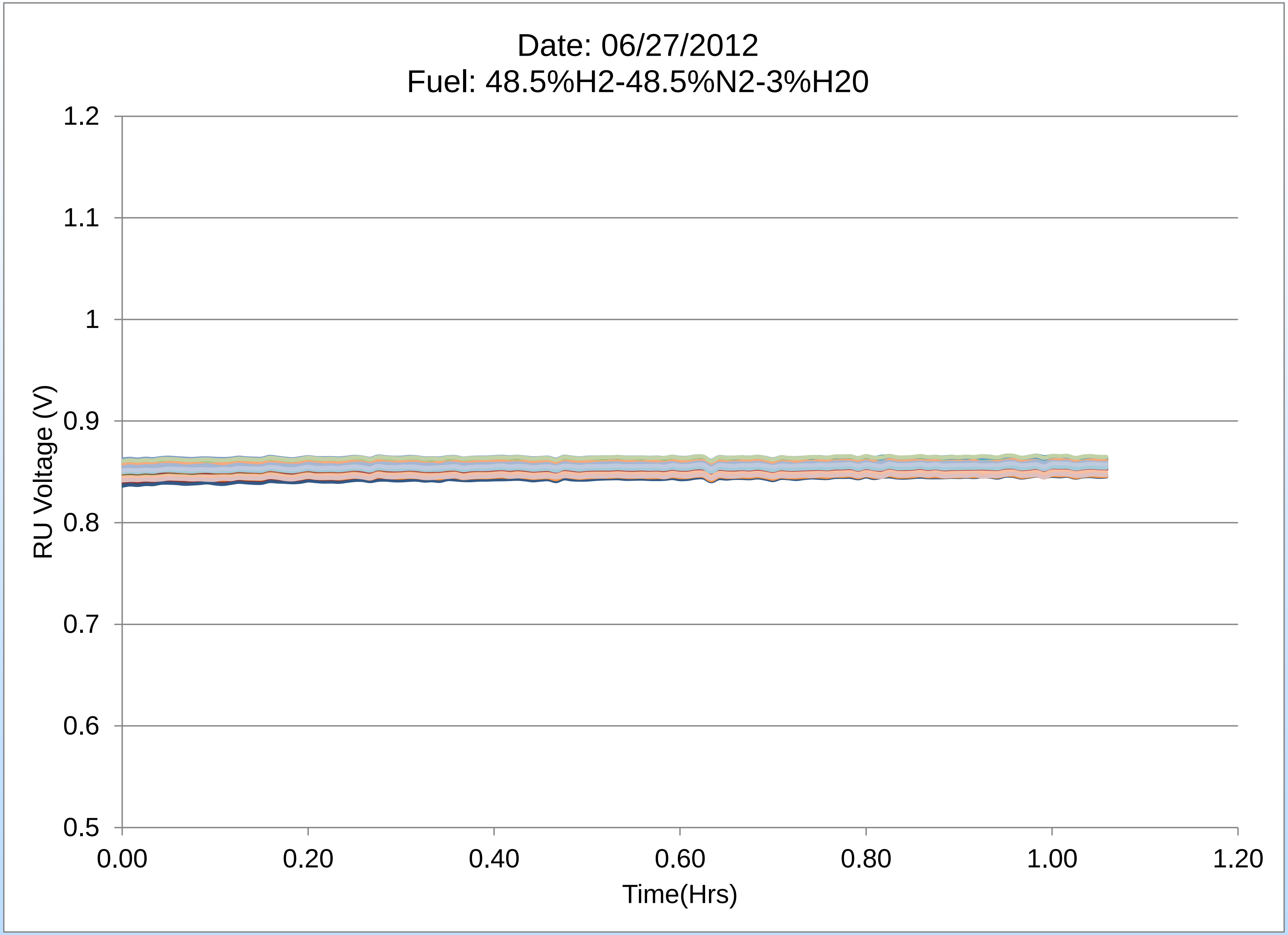


# MOST RECENT 38-CELL GEN 4 STACK INITIAL POLARIZATION VOLTAGE SPREAD




| Pressure (kPa) | Anode External (sccm) | Cathode External (sccm) | Cross (sccm) |
|---|---|---|---|
| 7.00 | 0.00 | 16.00 | 0.00 |

MOST RECENT 38-CELL GEN 4 STACK INITIAL CONSTANT CURRENT PERFORMANCE (0.35 A/$cm^2$)



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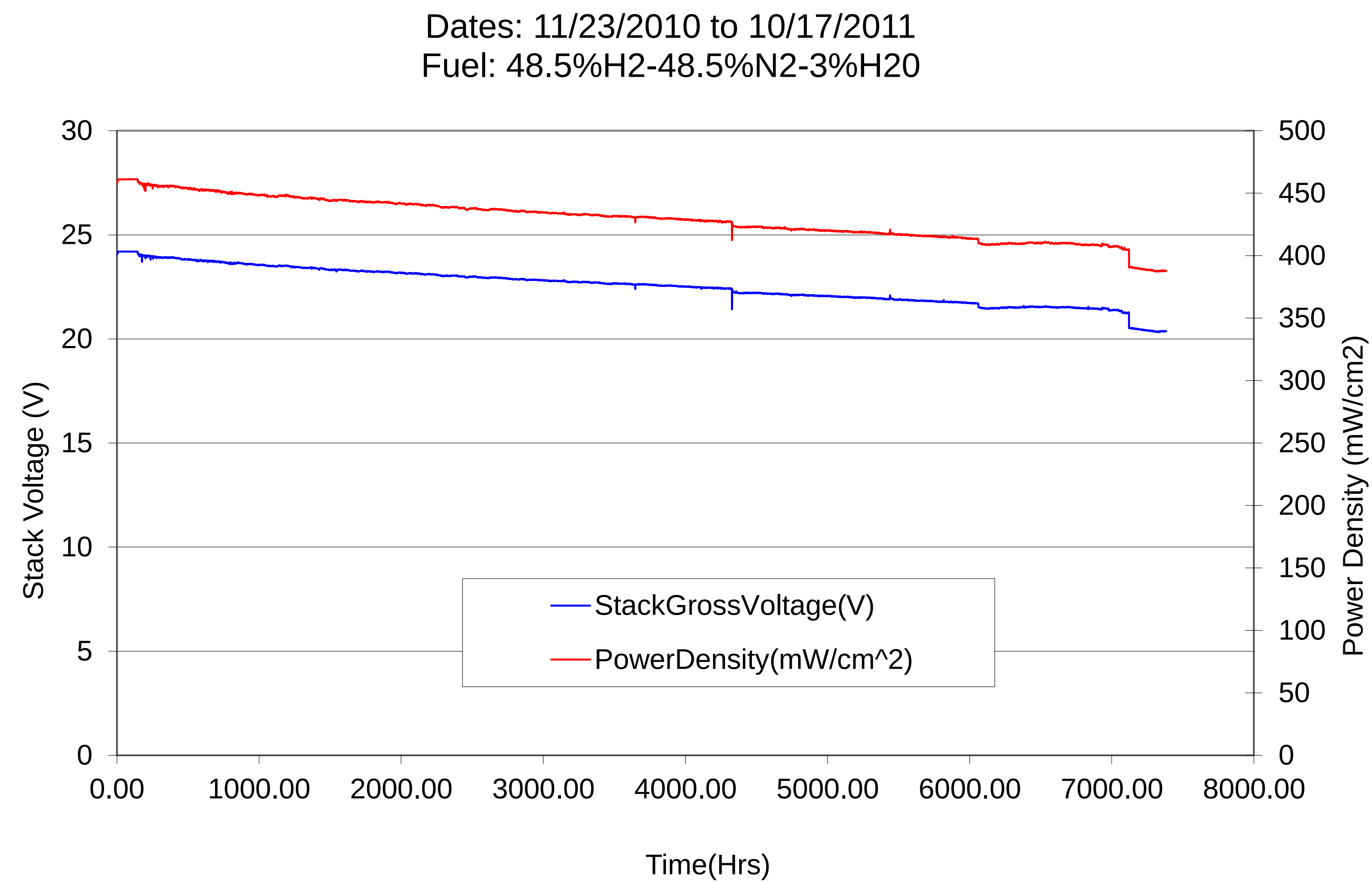
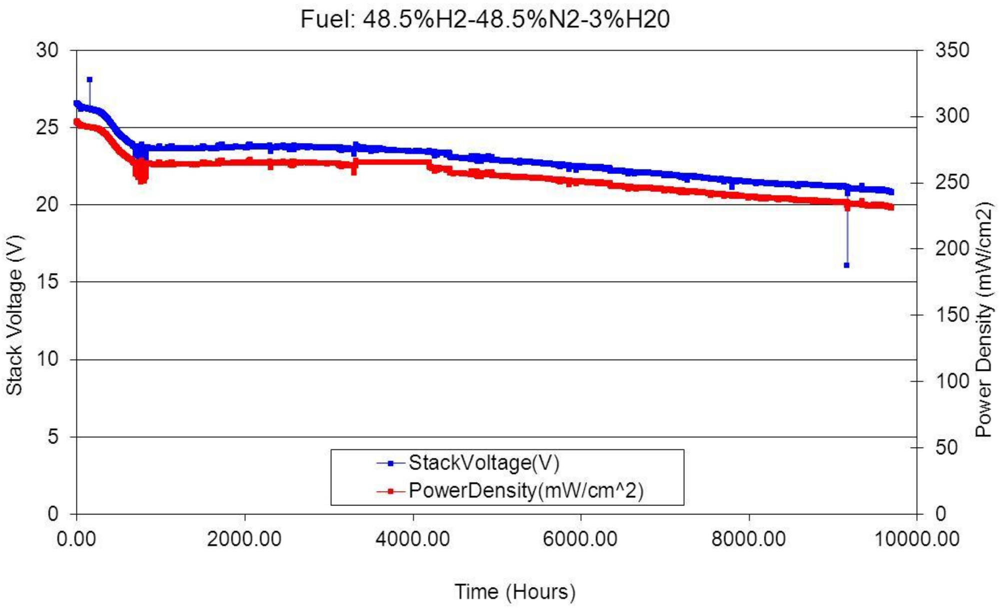
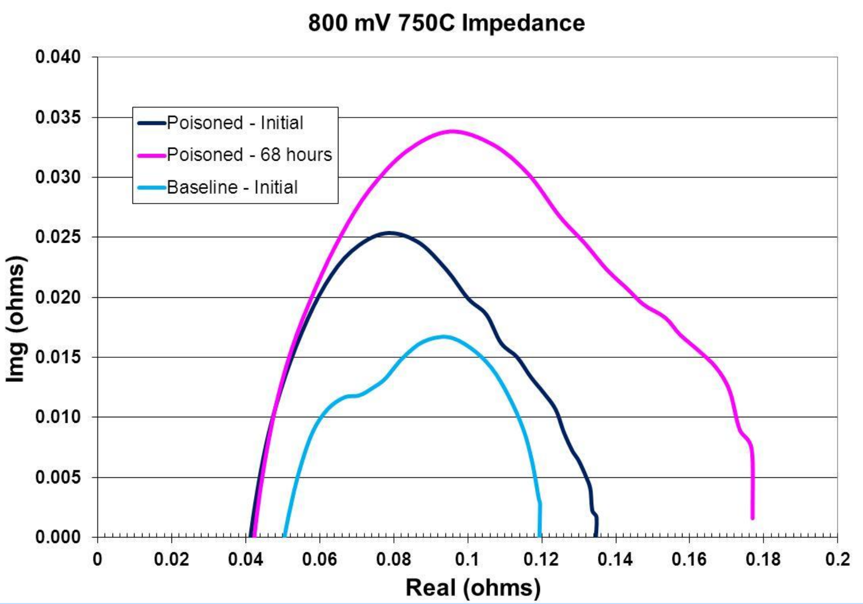
# GEN 3.2 STACK DURABILITY TESTING (0.57 A/cm$^2$)

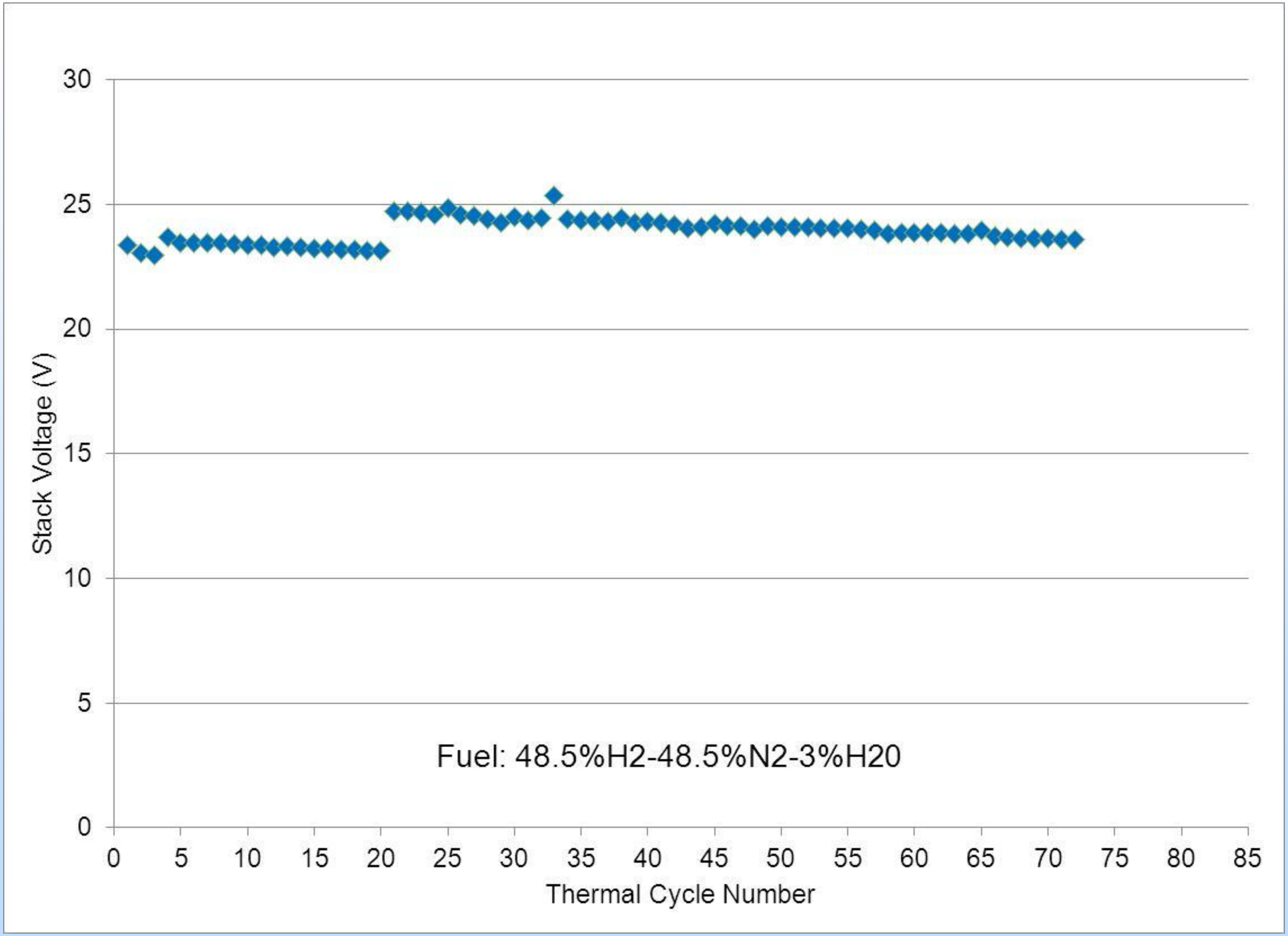


# GENERATION 3 30-CELL STACK DURABILITY



# 30-CELL GEN 4 STACK THERMAL CYCLING



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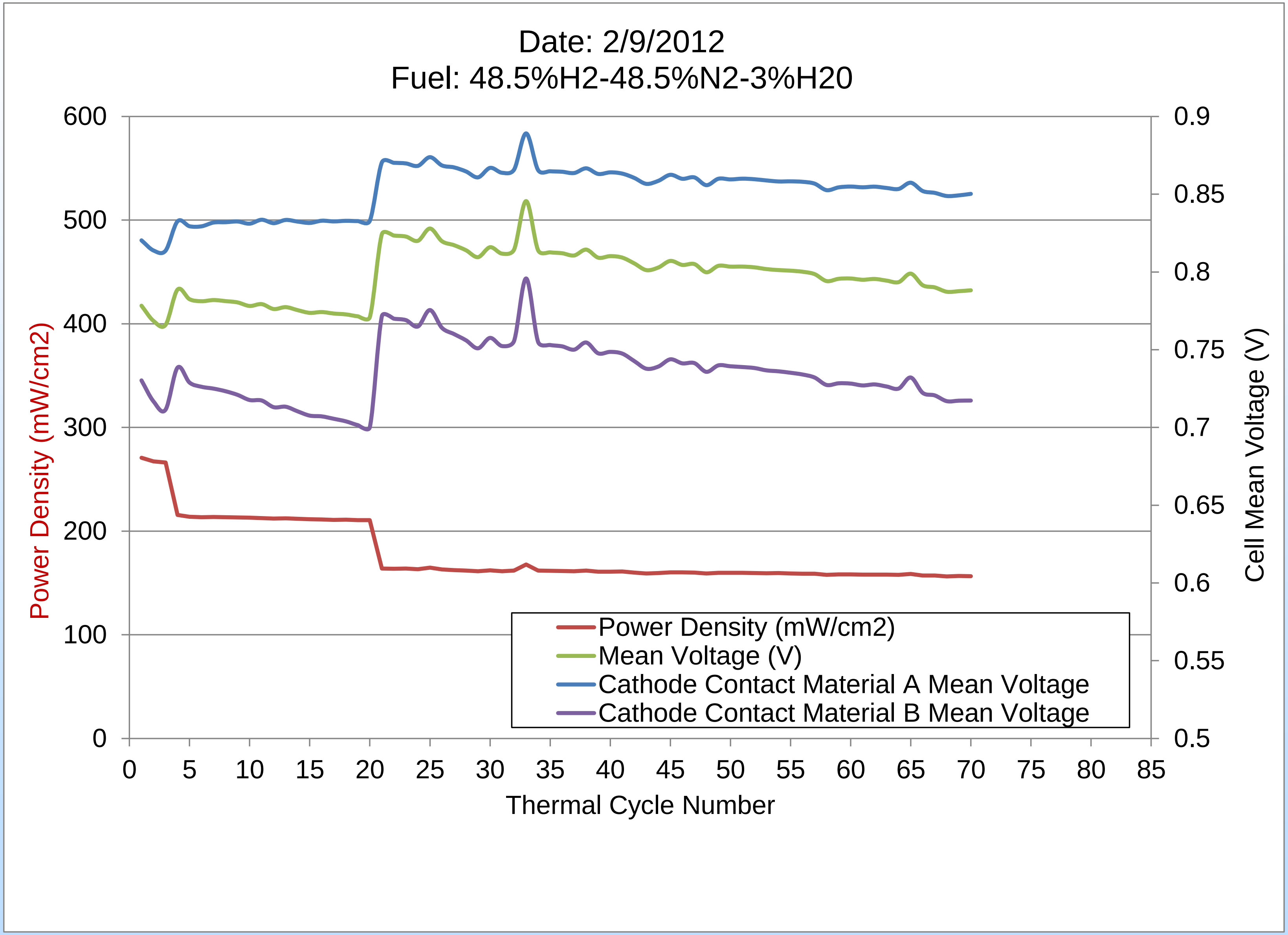
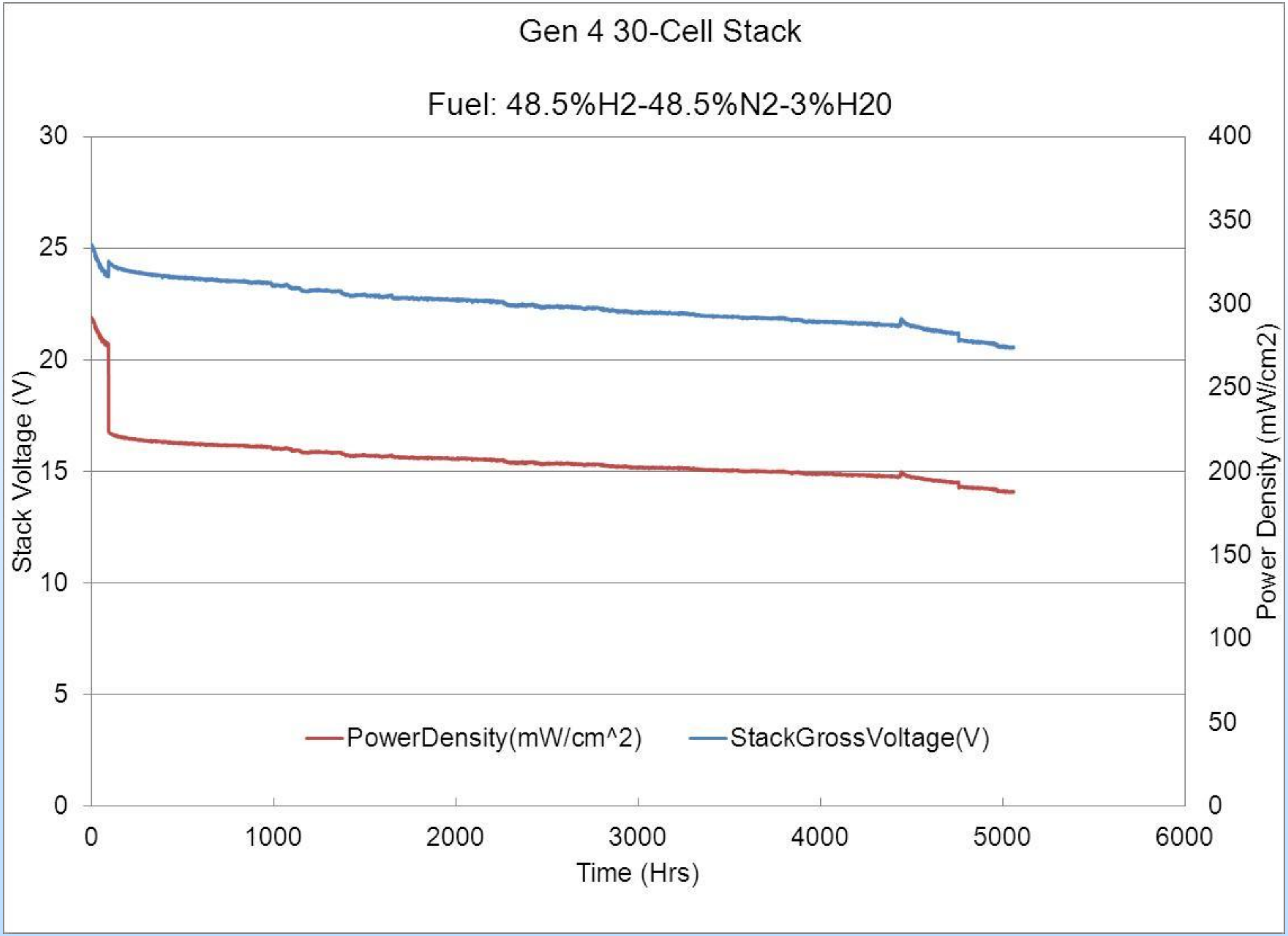
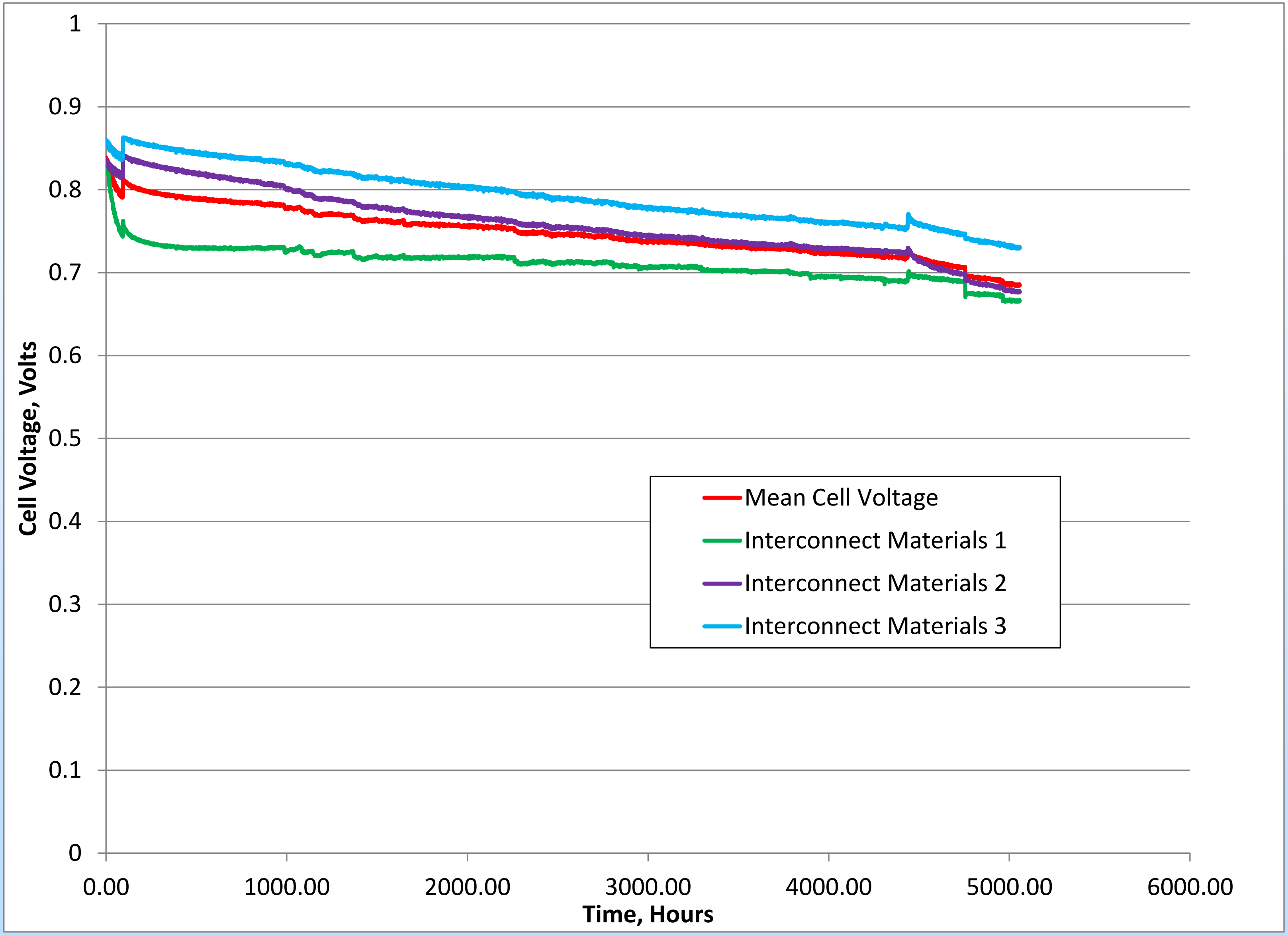
# THERMAL CYCLING CATHODE CONTACT MATERIALS



# 30-CELL GEN 4 STACK CONSTANT CURRENT DURABILITY (0.27 A/cm$^2$)



# INTERCONNECT MATERIAL PERFORMANCE



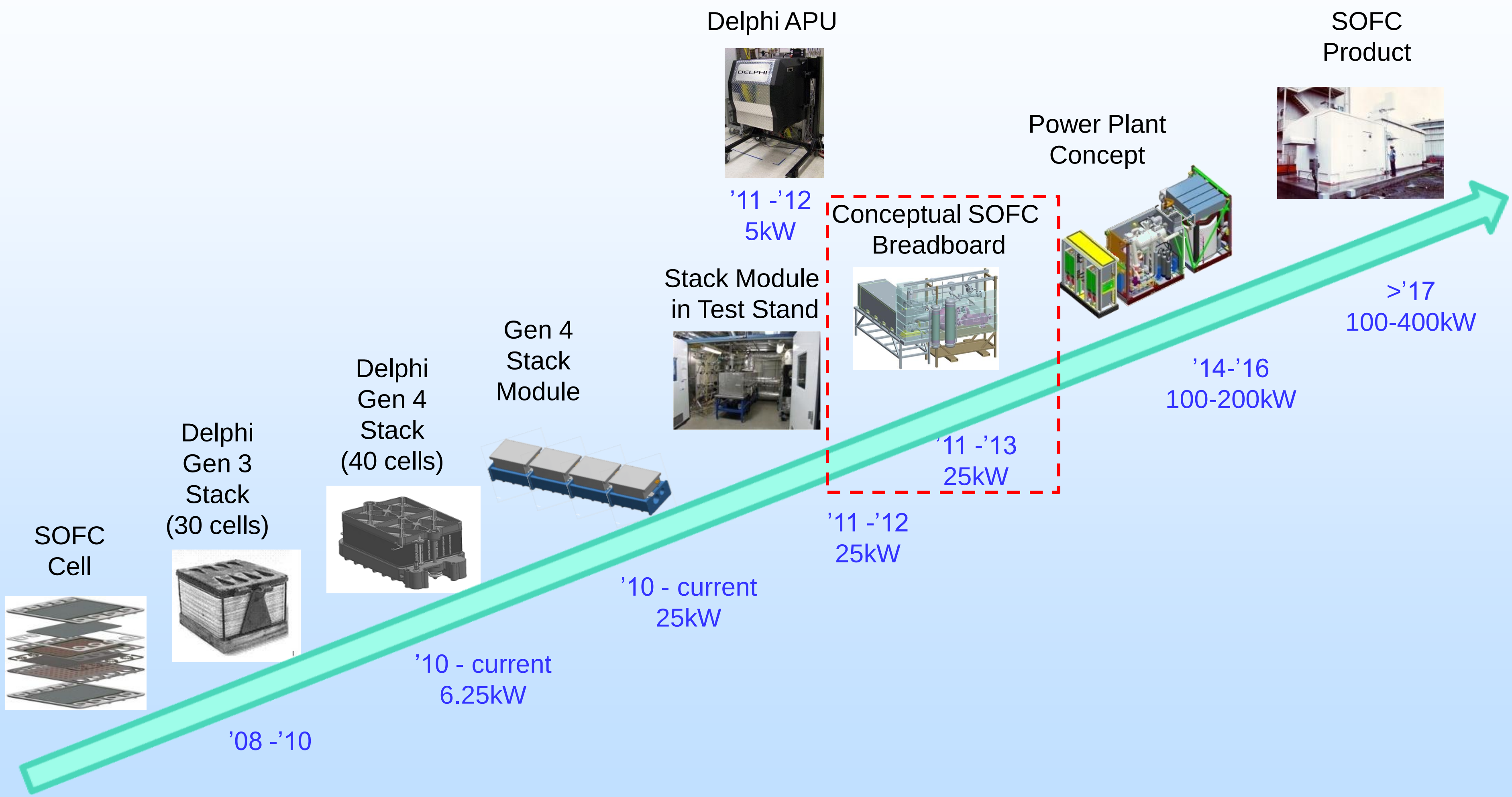
# UTC OBJECTIVES FOR PHASE II

- Design and build 15-25kW SOFC breadboard
- Make modifications to SOFC test stand from Phase I to test breadboard
- Perform extensive verification of test stand and breadboard on beater stack prior to start of endurance testing
- Demonstrate 1500 hours endurance on 4-stack module in a system construct (breadboard)
- Demonstrate thermally self-sustaining operation
- Demonstrate peak power operation

# SUMMARY HIGHLIGHTS - SYSTEM

- Demonstrated ~1,250 hours durability on Gen 4 stack module.
- Improved test stand reliability by ~3x to complete Phase I
- Completed conceptual and preliminary design for the 25kW breadboard
- Detailed design and breadboard build is ~80% complete
- Test stand modifications for Phase II are ~80% complete
- Software design and bench verification is 90% complete
- Ex-situ verification of breadboard fuel recycle assembly is underway
  - Completed ~100 hours of continuous durability at operating temperatures on an ex-situ test rig

# OVERVIEW – SOFC PRODUCT DEVELOPMENT ROADMAP



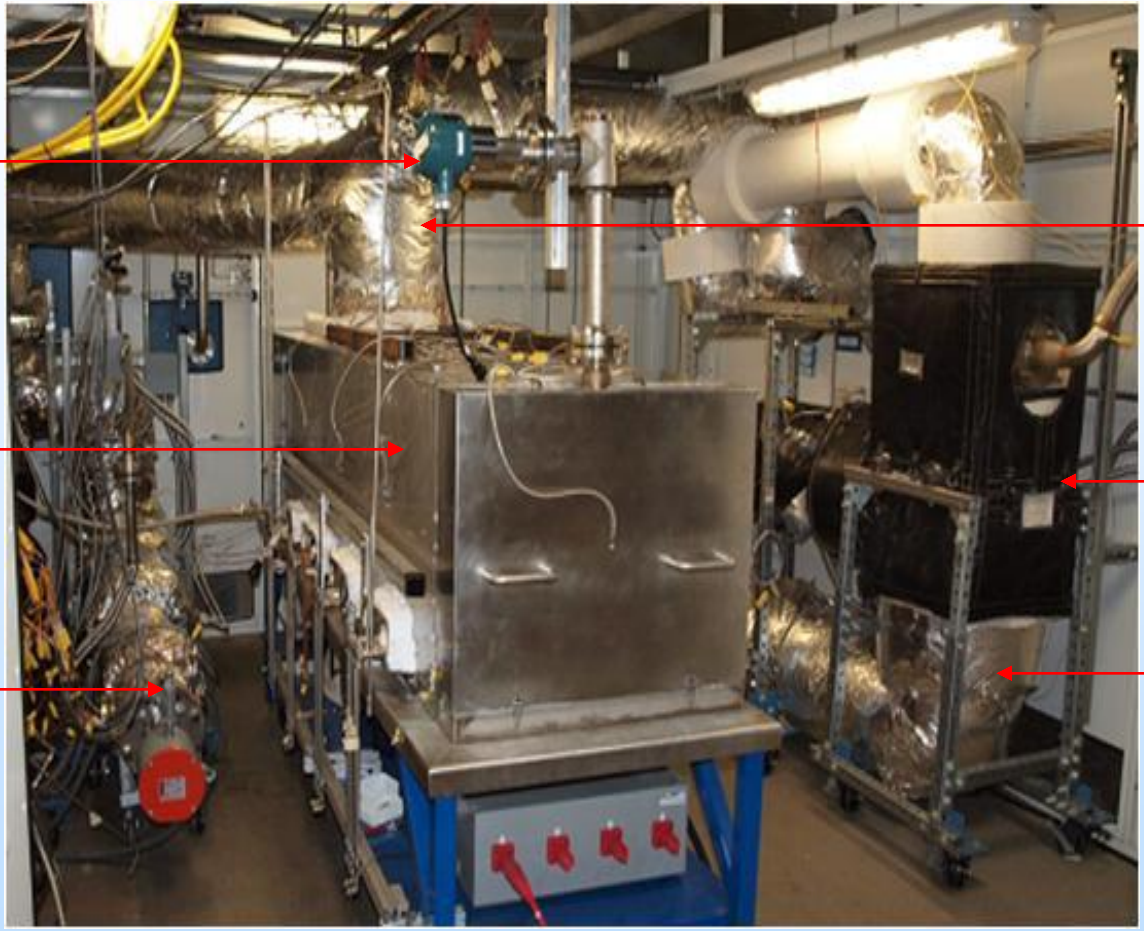
# TASK 6.3 - STACK MODULE ENDURANCE TESTING

## Stack Module

Hot Box
Safety Sensors

Stack Module
Hot Box

Fuel Inlet
Heaters



Gas Inlet/Exit

Cathode
Recuperative
Heat Exchanger

Air Inlet
Heater

Delphi Stack Module in the 50 kW capable
test stand at UTC Power

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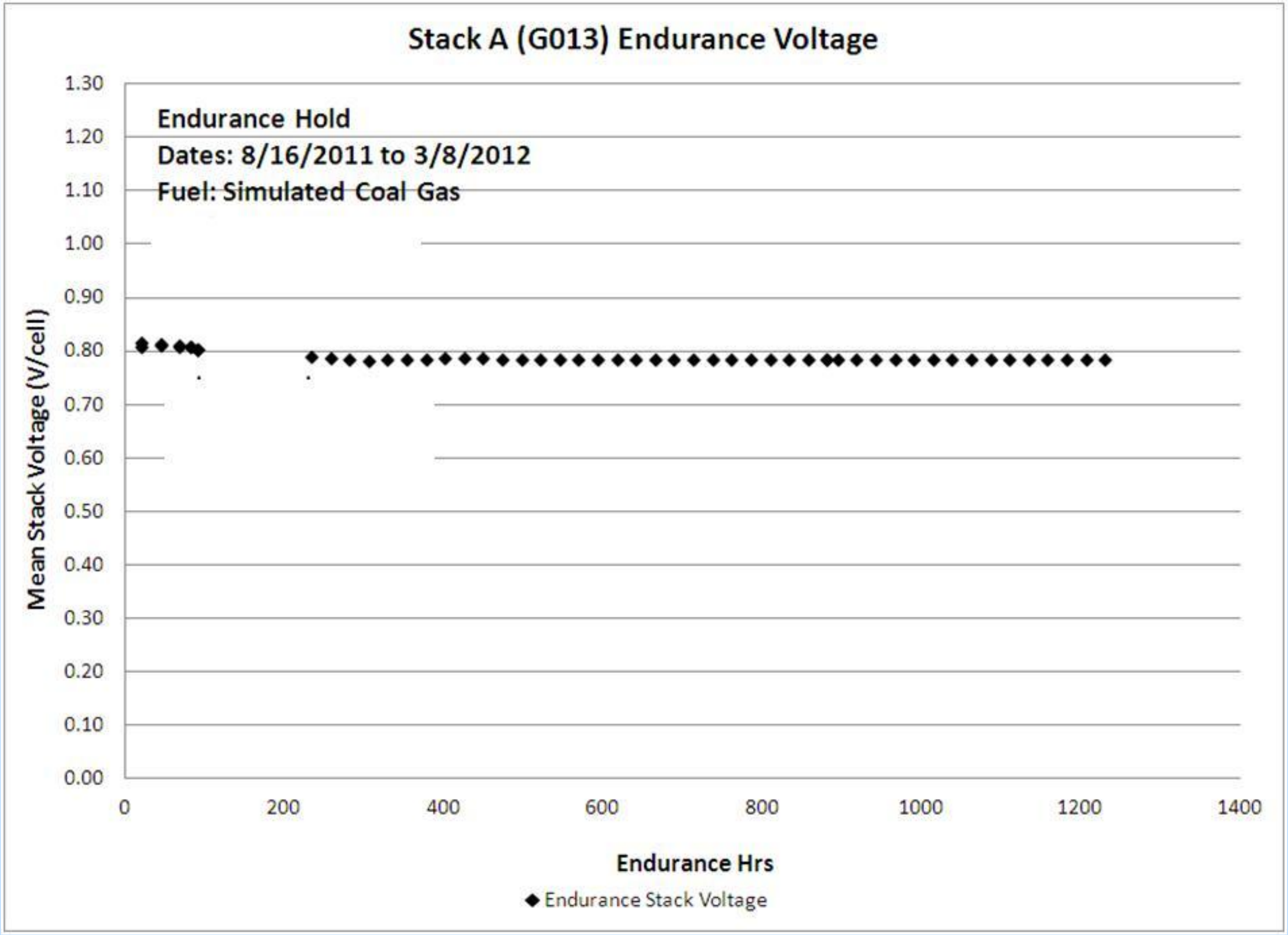
# TASK 6.3 - STACK MODULE ENDURANCE TESTING

## Phase I Stack Performance



# TASK 6.3 - STACK MODULE ENDURANCE TESTING

## Endurance Test – System Level Learning

- Completed fuel contaminant tests
- Completed cathode side chromium sampling
- Obtained data on stack manifold temperature distribution
  - Temperature data used to estimate stack heat loss for Phase II
- Obtained data on stack manifold pressure drop
  - Currently anode over cathode at stack exit; working with Delphi
- Improved test stand reliability

# TASK 4.1 - BREADBOARD/SYSTEM DESIGN

## NPD Gated Process for System Design and Development

**Conceptual Design**

✓Requirements Generation

✓Trade Studies

✓Conceptual Models

✓System Matches

✓Preliminary Physical Layout

**Preliminary Design**

✓Component Requirements Generation

✓Component Design

✓Controls Design

✓FMEA/FA/HA

✓Detailed Physical Layout

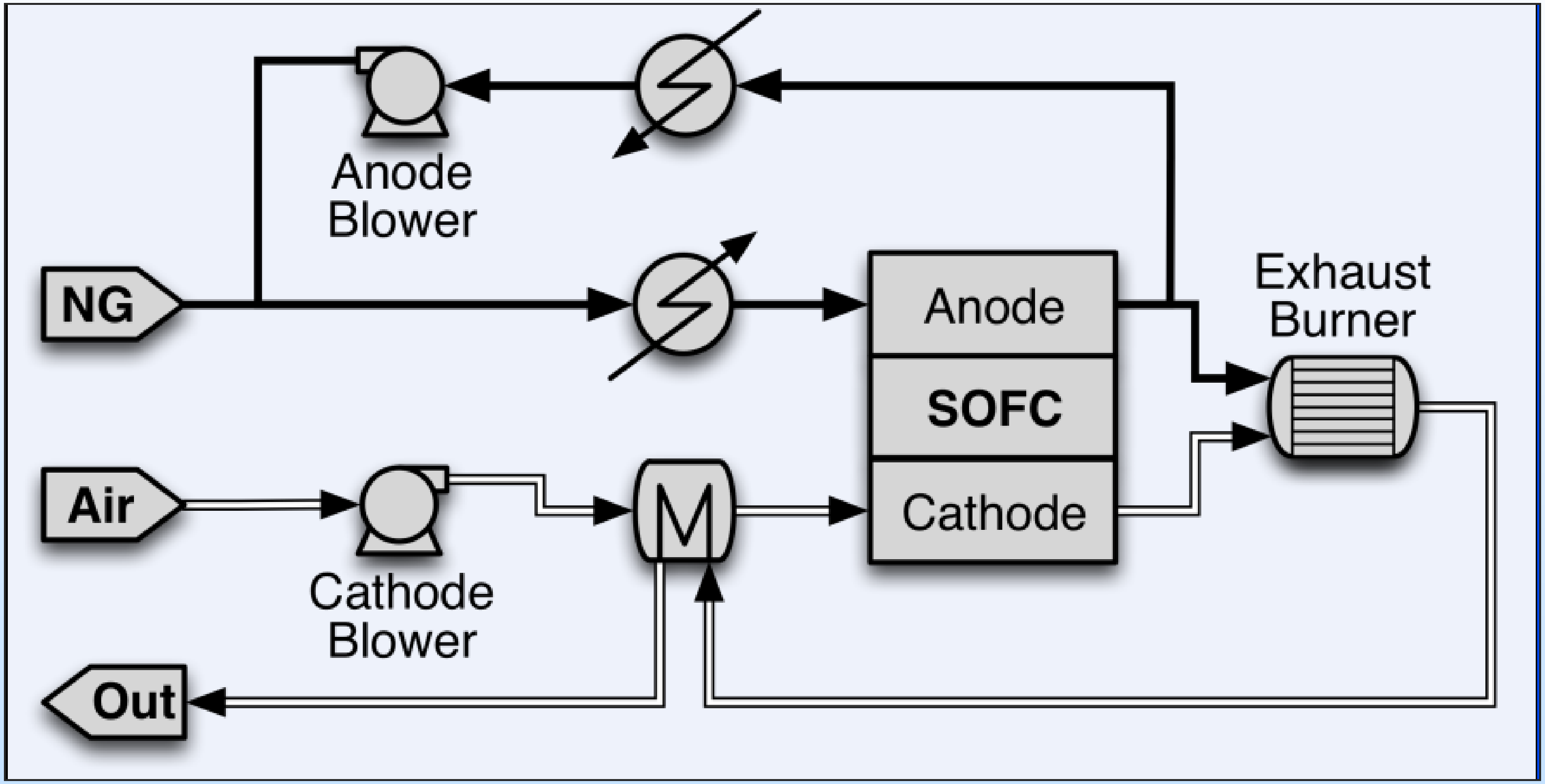
**Detailed Design/Test**

- Component Tests
- Hardware Build/Integration
- Test Plan Review
- Breadboard Checkouts
- Endurance Test

**Design Review** | **Design Review** | **Test Report**

# TASK 4.1 - BREADBOARD/SYSTEM DESIGN

## Breadboard Schematic




- Fuel recycle for maximizing efficiency
- HEXs for exhaust heat recovery
- Catalytic burner for exhaust management and heat up of cathode inlet air

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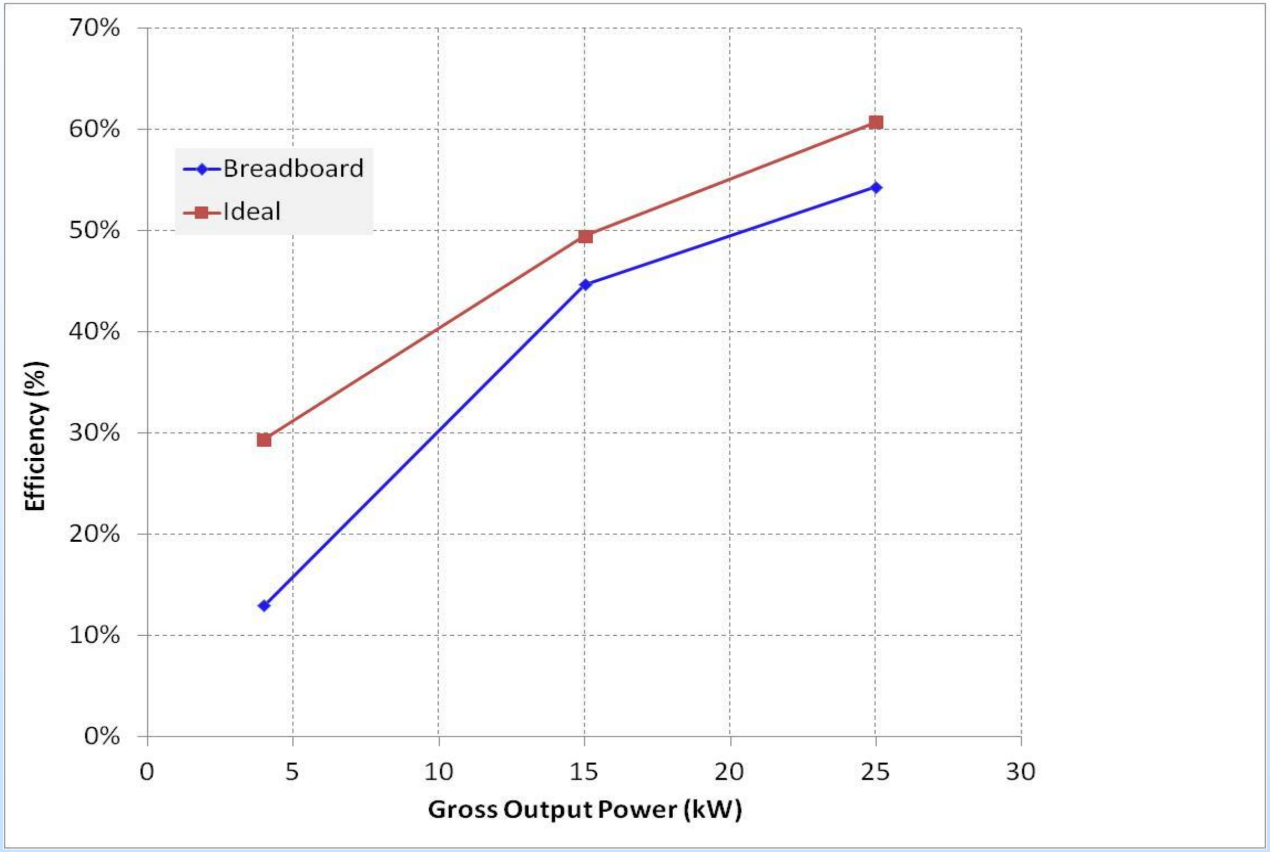
# TASK 4.1 - BREADBOARD/SYSTEM DESIGN

## Breadboard Projected Efficiency

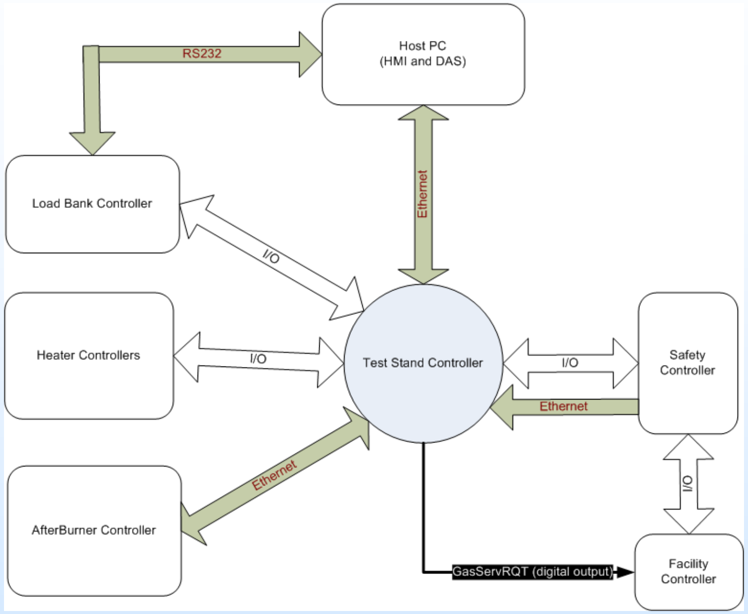



**Breadboard Projections vs. Ideal**

- Several BOP (recycle blower) over-sized
- Heaters included for contingency on breadboard; not required for a product
- Air blower for cathode supply not optimized

# TASK 4.1 - BREADBOARD/SYSTEM DESIGN

## Control Strategy




Test stand controller

- Controls breadboard startup sequence, transition to load, on-load operation and breadboard shutdown for product protection

Host PC & Data Acquisition

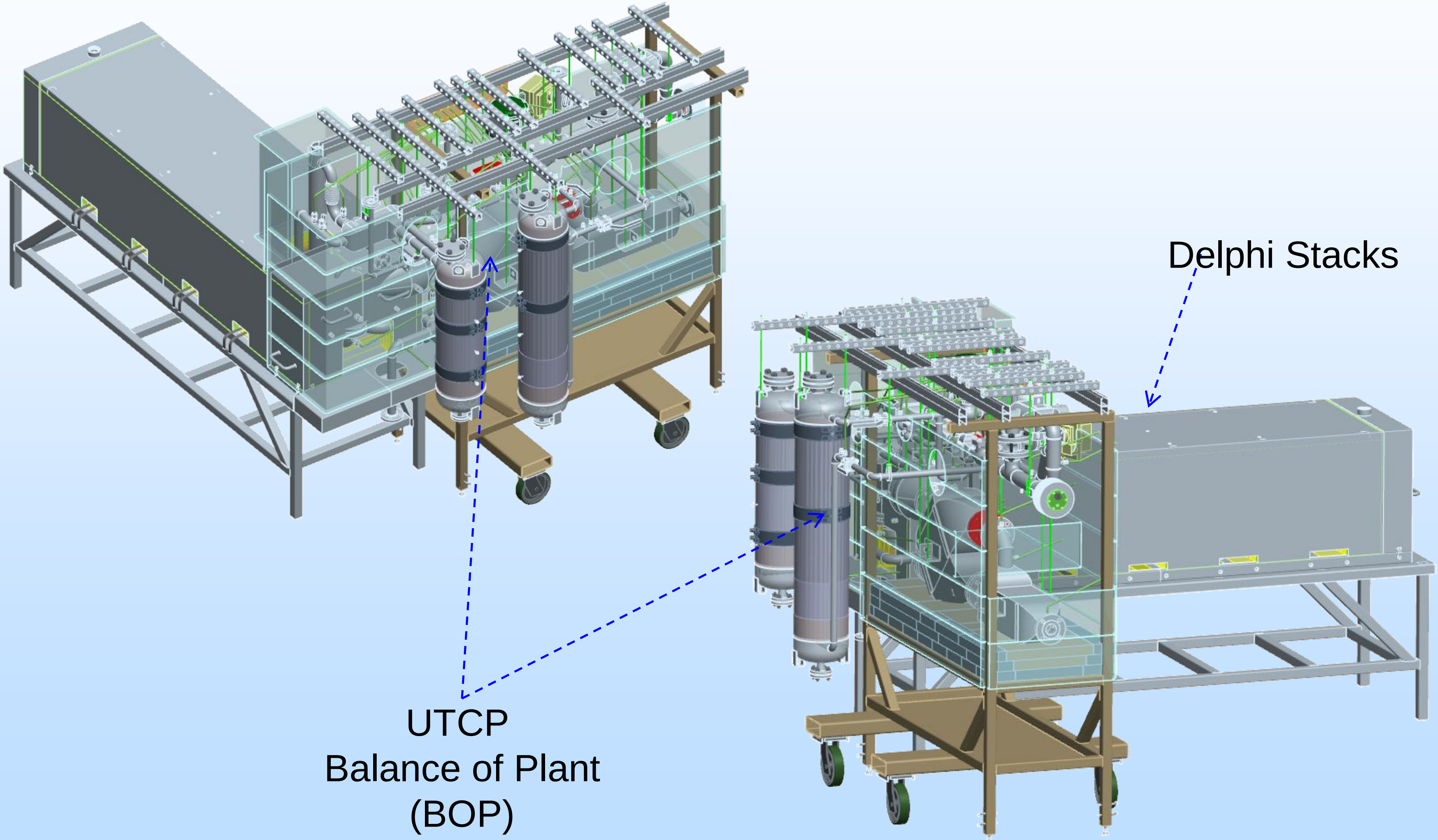
- GUI-based user interface for controlling test process, monitoring and data collection

### Other Controllers

1. Safety Controller
   - Hard-wired controls for safety and personnel protection
2. Facility Controller
   - Provides safety shutoff for all reactant supply system
3. After Burner Controller
   - Controls test stand afterburner
4. Heater controllers
   - Maintain test stand controller requested heater set point

# TASK 4.1 - BREADBOARD/SYSTEM DESIGN

## Breadboard Layout



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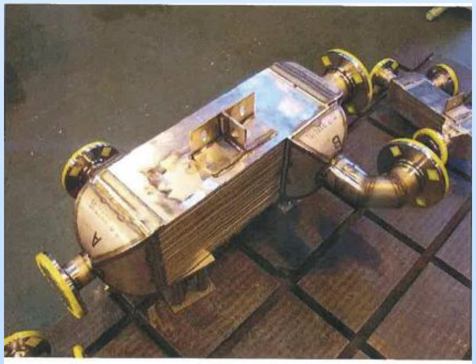
# TASK 4.1 - BREADBOARD/SYSTEM DESIGN

## Breadboard Design



**Fuel System Components**

**Air System Components**

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# TASK 4.1 - BREADBOARD/SYSTEM DESIGN

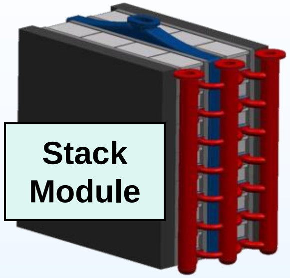
## Risk Mitigation: Ex-situ Blower Tests

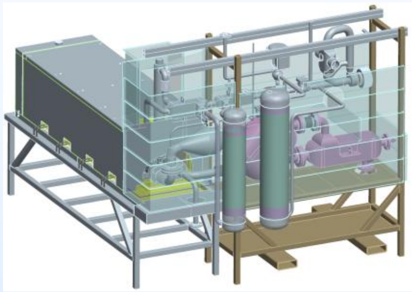
Test Rig for Blower Performance
and
Endurance Test

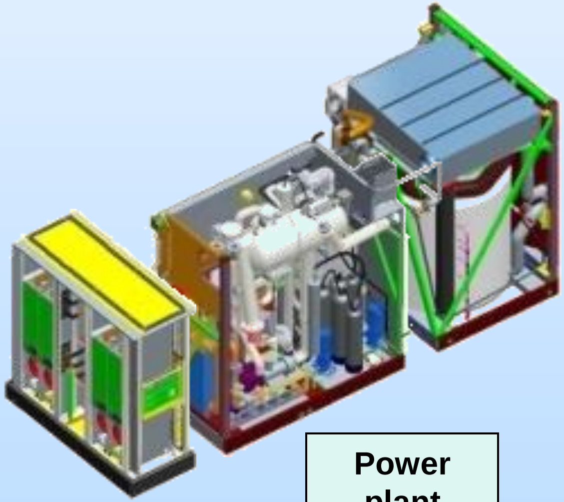
# FUTURE WORK

## Beyond Phase II

- Continue cost reduction of stack and power plant components
- Improve stack durability to meet SECA goals
- Demonstrate breadboard endurance
- Risk reduce for critical components: blowers, fuel processing components, catalytic burners
- Collect system level data for scaled-up power plant/prototype design in future phases



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